

TECHNICAL USER'S MANUAL FOR:

MICROSPACE[®]

PC/104 Peripheral boards

MSMF104

Flash-Card

#180599-1

DIGITAL-LOGIC[®]

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1 PREFACE

This manual is for integrators and programmers of systems based on the MicroSpace card family. It contains information on hardware requirements, interconnections, and details of how to program the system. The specifications given in this manual were correct at the time of printing; advances mean that some may have changed in the meantime. If errors are found, please notify DIGITAL-LOGIC AG at the address shown on the title page of this document, and we will correct them as soon as possible.

1.1 How to use this manual

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MicroSpace-PC. It provides instructions for installing and configuring the MSM104RS board, and describes the system and setup requirements.

1.2 Trademarks

Chips & Technologies	SuperState R
MicroSpace, MicroModule	DIGITAL-LOGIC AG
DOS Vx.y, Windows	Microsoft Inc.
PC-AT, PC-XT	IBM
NetWare	Novell Corporation
Ethernet	Xerox Corporation
DR-DOS, PALMDOS	Digital Research Inc. / Novell Inc.
ROM-DOS	Datalight Inc.

1.3 Disclaimer

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1.4 Who should use this product

- Electronic engineers with know-how in PC-technology.
- Without electronic know-how we expect you to have questions. This manual assumes, that you have a general knowledge of PC-electronics.
- Because of the complexity and the variability of PC-technology, we can't give any warranty that the product will work in any particular situation or combination. Our technical support will help you.
- Pay attention to the electrostatic discharges. Use a CMOS protected workplace.
- Power supply OFF when you are working on the board or connecting any cables or devices.

**This is a high technology product.
You need know-how in electronics and PC-technology to
install the system !**

1.5 Recycling Information

- Hardware:**
- **Print:** epoxy with glass fiber
wires are of tin-plated copper
 - **Components:** ceramics and alloys of gold, silver
check your local electronic recycling
- Software:** - **no problems:** re-use the diskette after formatting

1.6 Technical Support

1. Contact your local Digital-Logic Technical Support in your country.
2. Use Internet Support Request form on <http://www.digitallogic.ch> -> Support -> Support Request
3. Send a FAX or an E-mail to DIGITAL-LOGIC AG with a description of your problem.

DIGITAL-LOGIC AG
Technical Support Dept.
Nordstrasse 11/F
CH-4542 Luterbach (SWITZERLAND)

Fax: ++41-32 681 53 31
E-Mail: support@digitallogic.ch

Support requests will only be accepted with detailed informations about the product (BIOS-, Board-Version) !

1.7 Limited Warranty

DIGITAL-LOGIC AG warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original product purchaser and is not transferable.

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2 OVERVIEW

2.1 Ordering Information

MSMF104-2D	Dual Flashdisk socket for 2x DOC2000
MSMF104-2D&S05	Dual Flashdisk with 0.5Mb SRAM-Disk
MSMF104-2D&S2	Dual Flashdisk with 2Mb SRAM-Disk

2.2 General Information

BUS:

Standard:	PC/104
Size:	16Bit / 8Bit connected

Power Supply:

Power:	Working: 5Volt / 1W
--------	---------------------

Physical Characteristics:

Dimensions:	Length: 90mm
	Width: 96mm
	Height: 15mm

Operating Environment:

Relative humidity:	5 - 90% non condensing		
Vibration:	5 to 2000 Hz		
Shock:	10g		
Temperature:	Operating:	Standard version:	-25°C to +70°C
		Industry version:	-25°C to +85°C (ask DIGITAL-LOGIC AG)
	Storage:		-55°C to 85°C

2.3 Flashdisk sockets

Specifications:

Specification:	
1.Socket Window:	D8000 – D9FFFh, Size = 8k
2.Socket Window:	DA000 – DBFFFh, Size = 8k
Flashdisk:	M-Systems DOC2000
Power:	5 Volt +/- 5%
Temperature:	-25°C to +70°C operating

2.4 SRAM-Disk

Specification:

SRAM-Window:	DC000 - DCFFFh	Size = 4k
Capacity:	0.5, 1, 1,5, 2MByte	Batterybuffered
Pageselectaddress	2C0h	1 Byte
Driver:	in the BIOS Extension or as TSR Driver for DOS	

2.5 29F016/32 onboard soldered (optional)

Specification:

FDISK:	DD000 – DDFFFh	Size = 4k
Capacity:	2 / 4MByte	
Pageselectaddress	2C0h	1Byte
Driver:	in the BIOS Extension or as TSR Driver for DOS	

2.6 BIOS-Extension (optional)

Specification:

BIOS-Window:	DE000 - DFFFFh	Size = 8k
Capacity:	lowest 8k segment of a 29F010	
Device:	29F010 or 27C010	

Any information is subject to change without notice.

3 PC/104 BUS SIGNALS

AEN, output

Address Enable is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. **low = CPU Cycle , high = DMA Cycle**

BALE, output

Address Latch Enable is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. This signal is used so that devices on the bus can latch LA17..23. The SA0..19 address lines latched internally according to this signal. BALE is forced high during DMA cycles.

/DACK[0..3, 5..7], output

DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ0 through DRQ7). They are **active low**. This signal indicates that the DMA operation can begin.

DRQ[0..3, 5..7], input

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK/) line goes active. DRQ0 through DRQ3 will perform 8-Bit DMA transfers; DRQ5-7 are used for 16 accesses.

/IOCHCK, input

IOCHCK/ provides the system board with parity (error) information about memory or devices on the I/O channel. **low = parity error, high = normal operation**

IOCHRDY, input

I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of one clock cycle (67 nanoseconds). This signal should be held in the range of 125-15600ns. **low = wait, high = normal operation**

/IOCS16, input

I/O 16 Bit Chip Select signals the system board that the present data transfer is a 16-Bit, 1 wait-state, I/O cycle. It is derived from an address decode. /IOCS16 is **active low** and should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA. The signal is driven based only on SA15-SAO (not /IOR or /IOW) when AEN is not asserted. In the 8 Bit I/O transfer, the default transfers a 4 wait-state cycle.

/IOR, input/output

I/O Read instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is **active low**.

/IOW, input/output

I/O Write instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is **active low**.

IRQ[3 - 7, 9 - 12, 14, 15], input

These signals are used to tell the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is **raised from low to high**. The line must be held high until the microprocessor acknowledges the interrupt request.

/Master, input

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a /DACK.

/MEMCS16, input

MEMCS16 Chip Select signals the system board if the present data transfer is a 1 wait-state, 16-Bit, memory cycle. It must be derived from the decode of LA17 through LA23. /MEMCS16 should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA.

/MEMR input/output

These signals instruct the memory devices to drive data onto the data bus. /MEMR is active on all memory read cycles. /MEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMR, it must have the address lines valid on the bus for one system clock period before driving /MEMR active. These signals are **active low**.

/MEMW, input/output

These signals instruct the memory devices to store the data present on the data bus. /MEMW is active in all memory read cycles. /MEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMW, it must have the address lines valid on the bus for one system clock period before driving /MEMW active. Both signals are **active low**.

OSC, output

Oscillator (OSC) is a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle. OSC starts 100µs after reset is inactive.

RESETDRV, output

Reset Drive is used to reset or initiate system logic at power-up time or during a low line-voltage outage. This signal is active high. When the signal is active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the permanent Master.

/REFRESH, input/output

These signals are used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel. These signals are **active low**.

SAO-SA19, LA17 - LA23 input/output

Address bits 0 through 19 are used to address memory and I/O devices within the system. These 20 address lines, allow access of up to 1MBytes of memory. SAO through SA19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. LA17 to LA23 are not latched and addresses the full 16 MBytes range. These signals are generated by the microprocessors or DMA controllers. They may also be driven by other microprocessor or DMA controllers that reside on the I/O channel. The SA17-SA23 are always LA17-LA23 address timings for use with the MSCS16 signal. This is advanced AT96 design. The timing is selectable with jumpers LAXx or Saxe.

/SBHE, input/output

Bus High Enable (system) indicates a transfer of data on the upper byte of the data bus, XD8 through XD15. Sixteen-Bit devices use /SBHE to condition data-bus buffers tied to XD8 through XD15.

SD[O..15], input/output

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/O devices. DO is the least-significant Bit and D15 is the most significant Bit. All 8-Bit devices on the I/O channel should use DO through D7 for communications to the microprocessor. The 16-Bit devices will use DO through D15. To support 8-Bit device, the data on D8 through D15 will be gated to DO through D7 during 8-Bit transfers to these devices; 16-Bit microprocessor transfers to 8-Bit devices will be converted to two 8-Bit transfers.

/SMEMR input/output

These signals instruct the memory devices to drive data onto the data bus for the first MByte. /SMEMR is active on all memory read cycles. /SMEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMR, it must have the address lines valid on the bus for one system clock period before driving /SMEMR active. The signal is **active low**.

/SMEMW, input/output

These signals instruct the memory devices to store the data present on the data bus for the first MByte. /SMEMW is active in all memory read cycles. /SMEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMW, it must have the address lines valid on the bus for one system clock period before driving /SMEMW active. Both signals are **active low**.

SYCLK, output

This is a 8 MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 66% duty cycle. This signal should only be used for synchronization.

TC output

Terminal Count provides a pulse when the terminal count for any DMA channel is reached. The TC completes a DMA-Transfer. This signal is expected by the onboard floppy disk controller. Do not use this signal, because it is internally connected to the floppy controller.

/OWS, input

The Zero Wait State (/OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-Bit device without wait cycles, /OWS is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-Bit device with a minimum of one-wait states, /OWS should be driven active one system clock after the Read or Write command is active, gated with the address decode for the device. Memory Read and Write commands to an 8-Bit device are active on the falling edge of the system clock. /OWS is **active low** and should be driven with an open collector or tri-state driver capable of sinking 20mA.

12V +/- 5%

used only for the flatpanel supply and BIAS generation.

GROUND = 0V

used for the entire system.

VCC, +5V +/- 0.25V

separate for logic and harddisk/floppy supply.

3.1 Expansion Bus

The bus currents are as follows:

Output Signals:	IOH:	IOL:
D0 - D16	24 mA	24 mA
A0 - A23	24 mA	24 mA
MR, MW, IOR, IOW, RES, ALE, AEN, C14	24 mA	24 mA
DACKx, DRQx, INTx, PSx, OPW	24 mA	24 mA

Output Signals:	Logic Family:	Voltage:
Input Signals:	ABT-Logic ViH(min.) = 2.15 V	ABT-Logic ViI(max.) = 0.85 V

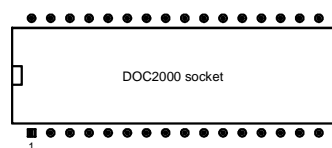
4 DETAILED SYSTEM DESCRIPTION

4.1 Installing the DiskOnChip (DOC2000)

On the SSD 36pin socket a DiskOnChip module from M-Systems may be installed with a capacity of 512k to 72MByte. This device is available from DIGITAL-LOGIC AG.

Operating Systems:

DOS, DL-DOS, RTX-DOS, WIN 3.11, ROM-WIN are working with these drives.
All other non DOS compatible systems need a driver.
Give attention to the pin 1 orientation in the 32pin SSD socket.



4.1.1 Enabling and Formatting of the DiskOnChip-Modules

Enabling:

Disable the Virus-Alert Option, and disable the DIGITAL-LOGIC flashdisk. On the BIOS V2.xx Setup, the M-Systems DOC2000 may be direct selected.

Format:

1. Boot-up from the standard floppydisk A: or from a harddisk.
2. Enter the tooldisk from M-Systems containing the format tool DFORMAT.EXE
The DFORMAT . EXE tool does not work under DL-DOS !
use: on DOC2000 V1.04 modules dformat /win:DE00 /S:DOC104.EXB /FIRST
use: on DOC2000 V1.05 modules dformat /win:DE00 /S:DOC105.EXB /FIRST
use: on DOC2000 V1.10 modules dformat /win:DE00 /S:DOC110.EXB /FIRST
" " " " " "
" " " " " "
3. Start format utility
The screen should inform about the status of the flashdisk.
4. Enter the DOS-Bootdisk and transfer the bootfiles with SYS A: C:
From this moment, the flashdisk is now the bootable drive C: and if any harddisk is conected it changes to letter D: and E:

For further informations about the DOC2000 please see the following manual as pdf on our CD !
flashdisk/doc2000/doc-util.pdf

4.2 *Installing the SRAM-DISK*

NOT AVAILABLE ON THIS BOARD AT THE MOMENT

5 CONNECTORS ON THE BOARD

PC/104 BUS Interface

Pin	A:	B:	C:	D:
0			Ground	Ground
1	IOCHCK	Ground	SBHE	MEMCS16
2	SD7	RESET	LA23	IOCS16
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	NC	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ13
7	SD2	(-12V)	LA18	IRQ14
8	SD1	NC	LA17	DACK0
9	SD0	+12V	MEMR	DRQ0
10	IOCHRDY	Ground	MEMW	DACK5
11	AEN	SMEMW	SD8	DRQ5
12	SA19	SMEMR	SD9	DACK6
13	SA18	SIOW	SD10	DRQ6
14	SA17	SIOR	SD11	DACK6
15	SA16	DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 Volt
17	SA14	DACK1	SD14	MASTER
18	SA13	DRQ1	SD15	Ground
19	SA12	REF	Ground	Ground
20	SA11	SYSCCLK		
21	SA10	IRQ7		
22	SA9	IRQ		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5 Volt		
30	SA1	OSC		
31	SA0	Ground		
32	Ground	Ground		

Attention:

Only the 8-Bit PC/104 Signals are used.

6 JUMPER LOCATIONS ON THE BOARD

6.1 The Jumpers on this MICROSPACE product

6.1.1 Memory-Adress Selection

SEL1	SEL2		
J3	J4		
close = '0'	open = '0'	D0xxxx – D7FFF	*
open = '1'	open = '0'	D8xxxx - DFFFF	

* Default

Device:	Size:	SEL1 = open (default)	SEL1 = close
DOC2000 Socket 1	8k	D0000 – D1FFF	D8000 – D9FFF
DOC2000 Socket 2	8k	D2000 – D3FFF	DA000 – DBFFF
SRAM-DISK	4k	D4000 – D4FFF	DC000 – DCFFF
FDISK onboard	4k	D5000 – D5FFF	DD000 – DDFFF
BIOS-Device	8k	D6000 – D7FFF	DE000 – DFFFF
Buffer for internal Databus	32k	D0000 – D7FFF	D8000 – DFFFF

6.1.2 Memory-Pageset I/O-Adress Selection

SEL3	SEL4		
J5	J6		
close = '1'	open = '0'	2D0	
open = '0'	open = '0'	2C0	*

* Default

Device:	Size:	SEL1 = closed	SEL1=open (default)
Low-Byte 273L	1Byte	2D0	2C0
High-Byte 273	1Byte	2D1	2C1

6.2 The part schematics of the MSMF104-2D

